SPECIFICATION AMENDMENT

Please amend paragraph [0037] as follows:

[0037] Bias voltages may also be generated. Bias VBN is applied to the gate of n-channel limiting transistor 44. The bias voltage VBN is usually set to be the same potential as the power rail, VDD (such as 1.8V) so that when a high voltage (3.3V) is applied to the I/O pad, the potential across the gate oxide in the Drain/Gate overlap region of n-channel transistor 44 is still well within the safe operating voltage region of the gate oxide. Since the voltage at the intermediate node NIN is VDD Vtn, this voltage drop across limiting ~~transistor 46~~ transistor 44 protects driver ~~transistor 46~~ transistor 42 from damage.